Claims

[c1] What is claimed is:

1.A chip-packaging with bonding options having a plurality of package substrates, comprising:

a first package substrate;

a second package substrate;

a chip mounted on first package substrate, the chip comprising a plurality of the bonding pads, one bonding pad being connected to the first package substrate, another bonding pad being connected to the second package substrate; and

a lead frame connected to one bonding pad.

[c2] 2.The chip-packaging of the claim 1 wherein the first package substrate is applied to a high voltage or a low voltage and the second package substrate is applied to a high voltage or a low voltage.

[c3] 3.The chip-packaging of the claim 2 wherein the high voltage is the voltage of the power supply and the low voltage is the ground voltage.

[c4] 4.The chip-packaging of the claim 1 wherein the lead frame is connected to one pin of the chip-packaging.

[c5] 5.The chip-packaging of the claim 4 wherein the pin is connected to a high voltage, a low voltage, or an input/output signal.

[c6] 6.The chip-packaging of the claim 1 wherein the first package substrate and the second package substrate have different voltages.

[c7] 7.The chip-packaging of the claim 1 wherein the first package substrate extends outside the chip and the second package substrate surrounds the chip.

[c8] 8.The chip-packaging of the claim 1 wherein the first package substrate and the second package substrate substantially approximate each of a plurality of the bonding pads.

[c9] 9.A chip-packaging method of utilizing a plurality of package substrates for a bonding option, comprising:
providing a first package substrate and a second package substrate;
mounting a chip on the first package substrate, the chip comprising a plurality of the bonding pads;
connecting one bonding pad to the first package substrate and connecting another bonding pad to the second package substrate; and
connecting one bonding pad to a lead frame.

[c10] 10.The chip-packaging method in claim 9 further comprising connecting the first package substrate to a high voltage or a low voltage.

[c11] 11.The chip-packaging method in claim 9 further comprising connecting the second package substrate to a high voltage or a low voltage.

[c12] 12.The chip-packaging method in claim 11 wherein the high voltage is the voltage of the power supply and the low voltage is the ground voltage.

[c13] 13.The chip-packaging method in claim 10 wherein the high voltage is the voltage of the power supply and the low voltage is the ground voltage.

[c14] 14.The chip-packaging method in claim 10 further comprising connecting the lead frame to a pin of the chip-packaging.

[c15] 15.The chip-packaging method in claim 14 further comprising connecting the pin to a high voltage, a low voltage, or an input/output signal.

[c16] 16.The chip-packaging method in claim 10 wherein the first package substrate and the second package substrate have different voltages.

[c17] 17.The chip-packaging method in claim 10 wherein the first package substrate extends outside the chip and the second package substrate surrounds the chip.

[c18] 18.The chip-packaging method in claim 10 wherein the first package substrate and the second package substrate substantially approximate each of a plurality of the bonding pads.